D D4811 Pages: 2

Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018

Course Code: EC206

Course Name: COMPUTER ORGANISATION (EC)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1 a) Express $(-18.125)_{10}$ in IEEE 754 single-precision floating point format. (3)

b) What is the use of a carry propagate adder? Design a 32-bit carry propagate adder. (5)

c) What are the 4 design principles of MIPS architecture? Explain (7)

2 a) Design a 3- bit equality comparator (3)

b) Design and implement hardware for a 4-bit logical shift right circuit. (4)

c) List out the functions performed by an ALU. Design an ALU using adder, inverter, multiplexer blocks and basic digital gates. (8)

3 a) List the 3 MIPS instruction formats with examples. (3)

b) With a diagram explain the R- type machine instruction format (5)

c) With a diagram explain the R- type machine instruction format (7)

Translate the following I-type assembly instruction into machine code.

lw $s3, -24($s4). Write the instruction in hexadecimal.

Hint: [$s3 and $s4 are registers 19 and 20, respectively.]

[*lw* has an opcode of 35.]

PART B

Answer any two full questions, each carries 15 marks

4 a) What are the different processes required to translate a program from a high-level language into machine language and executing it? Explain. (7)

b) What are the 3 state elements of multi cycle MIPS processor? Explain each with diagram (8)

5 a) Define Pseudo instruction and write MIPS instruction for the following pseudo instructions (5)

i) clear $t0 ii) nop

b) Explain about the different addressing modes in MIPS. (10)

6 a) Draw datapath for single cycle implementation for R-type instructions along with (10)

central signals. Explain clearly.

b) What are the 3 advantages of multi cycle processor over single cycle processor? (5)

PART C

Answer any two full questions, each carries 20 marks

7 a) Define Miss Rate, Hit Rate and Average memory access time. (6)

b) What is meant by ROM? Explain the various types of ROM. (4)

c) Explain with a diagram how virtual memory address is translated to physical address using page table. (10)

8 a) Explain the working of DRAM and SRAM with neat diagram. (10)

b) Explain the various data transfer methods. (10)

9 a) Explain direct mapping in cache memory with diagram. (8)

b) What are the write policy classifications of cache memory? Explain. (6)

c) What is the role of TLB (Translation Look aside Buffer) in virtual address translation? (6)

****