Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree (S,FE) Examination August 2021 (2015 Scheme)

Course Code: EC206

Course Name: COMPUTER ORGANISATION (EC)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1 a) Illustrate the basic functional units of a computer and list the functions of each unit. (6)

b) Design and implement a 1-bit ALU that will perform the following arithmetic and logical operations. Only one adder should be used for both add (+) and sub (-) operation. (9)

$F_{2:0}$	Function
100	NOT b
001	a AND b
010	a OR b
011	a + b
111	a - b

2 a) Explain the R-type and I-type instruction formats in MIPS with example. (5)

b) Identify the type of instructions given. Also write the operation performed when each instruction is executed. (10)

(a) add $t1, $s4, $s5

(b) addi $t3, $s3, -12

(c) lw $t0, 35($t0)

(d) sw $s1, 9($t1)

3 a) Discuss about operands and registers of MIPS processor. (6)

b) With examples, differentiate logical shifter, Arithmetic shifter and Rotator. Design and Implement 4-bit logical shift right circuit. (9)

PART B

Answer any two full questions, each carries 15 marks

4 a) Explain the five addressing modes of MIPS with example. (15)

5 a) Differentiate between single-cycle micro architecture and multi-cycle microarchitecture. (5)

b) Draw the datapath for single cycle processor for *add* instruction. (10)

6 a) How does a multicycle processor address the three weaknesses of single-cycle processor? (7)

b) With neat diagram explain MIPS Memory Map (8)

PART C

Answer any two full questions, each carries 20 marks

7 a) Describe the role of translation look aside buffer in address translation. (7)

b) Explain why refreshing is essential in DRAM and not required in SRAM. (4)

c) Describe programmed I/O and Interrupt driven I/O. (9)

8 a) Differentiate between the two write policies in cache memory. (5)

b) Draw the memory hierarchy diagram. (5)

c) Illustrate how data is found in a direct mapped cache. (10)

9 a) Explain the principle of cache memory and the terms used in cache memory (8)

b) Draw the internal organization of a SRAM cell and explain the read and write operation. (7)

c) Explain DMA data transfer method. (5)

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